WHAT IS CLAIMED IS:

1. A semiconductor device, comprising:

a memory cell array having a plurality of cell units;

a bit line amplifier for amplifying a voltage difference between a bit line voltage and a complementary bit line voltage of the memory cell array;

switching devices activated by a column selection line signal for electrically connecting a data line and a complementary data line to the bit line and the complementary bit line, respectively; and

a write driver for supplying a write data voltage to the data line and the complementary data line,

wherein the column selection line signal is generated during a write recovery time.

2. The semiconductor device as claimed in claim 1, wherein the column selection line signal is repetitively generated during the write recovery time.

3. The semiconductor device as claimed in claim 2, further comprising a signal generator for generating the column selection line signal,

wherein the signal generator is activated by a signal derived from an AND operation of an AND gate with respect to a column selection line enable signal and a column address selection signal activated by a column address signal and is deactivated by a column selection line disable signal, for generating the column selection line signal.

4. The semiconductor device as claimed in claim 3, wherein the column selection disable signal is generated after the column selection line enable signal is generated.

5. The semiconductor device as claimed in claim 4, wherein the column selection line disable signal is generated with a delay by at least half of the period of the column selection

line enable signal, compared to the column selection line enable signal.

6. The semiconductor device as claimed in claim 3, wherein the signal generator comprises:

a first PMOS transistor into which a signal, derived from an AND operation of an AND gate with respect to the column selection line enable signal and the column address selection signal, is input;

an NMOS transistor into which the signal derived from the AND operation of the AND gate with respect to the column selection line enable signal and the column address selection signal is input;

a second PMOS transistor connected between the first PMOS transistor and the NMOS transistor and into which an inverted signal of the column selection line disable signal is input; and

an inverter connected to a point between the second PMOS transistor and the NMOS transistor.

7. The semiconductor device as claimed in claim 6, wherein the signal generator further comprises a second inverter connected to the inverter via a latch.

8. The semiconductor device as claimed in claim 3, wherein the column selection line enable signal is generated by an AND operation of an AND gate with respect to the write enable signal and a master clock signal.

9. The semiconductor device as claimed in claim 3, wherein the column selection line disable signal is generated by an AND operation of an AND gate with respect to the master clock signal after a predetermined delay time and the write enable signal activated by an inverted signal of the master clock signal.

10. The semiconductor device as claimed in claim 1, further comprising a signal generator for generating the write enable signal,

wherein the signal generator is activated by a write command signal and is deactivated by a stop signal of a column address burst counter.

11. The semiconductor device as claimed in claim 10, wherein the signal generator comprises:

a first NOR gate into which the write command signal is input;

a second NOR gate connected to the first NOR gate via a latch and into which the stop signal of the column address burst counter is input; and

an inverter connected to an output terminal of the first NOR gate.

12. The semiconductor device as claimed in claim 10, wherein the stop signal of the column address burst counter is generated with a delay by at least one clock of a master clock signal after a start of the write recovery time.

13. The semiconductor device as claimed in claim 12, wherein the stop signal of the column address burst counter is generated with a delay in proportion to a value of the write recovery time.

14. The semiconductor device as claimed in claim 13, wherein the stop signal of the column address burst counter is activated by a write recovery time enable signal.

15. The semiconductor device as claimed in claim 14, further comprising a signal generator for generating the write recovery time enable signal,

wherein the signal generator comprises:

a PMOS transistor into which an inverted signal of a write recovery time determination signal is input;

an NMOS transistor into which the inverted signal of the write recovery time

determination signal is input;

a fuse connected between the PMOS transistor and the NMOS transistor; and

an inverter connected to a connection point between the fuse and the NMOS transistor.

16. The semiconductor device as claimed in claim 15, wherein the signal generator further comprises a second inverter connected to the inverter via a latch.

17. The semiconductor device as claimed in claim 3, wherein an internal column address signal is generated after the column address signal is generated after a predetermined delay time.

18. The semiconductor device as claimed in claim 17, wherein the column address signal is reset by the stop signal of the column address burst counter.

19. The semiconductor device as claimed in claim 18, wherein the column address signal is activated by a column address set signal and is generated after the predetermined delay time.

20. The semiconductor device as claimed in claim 19, wherein the column address signal is activated by a signal derived from an AND operation of an AND gate with respect to the master clock signal and an inverted signal of the column address set signal and the internal column address signal is generated.

21. The semiconductor device as claimed in claim 20, wherein the column address signal is generated during at least one clock of the master clock signal after a start of the write recovery time.

22. The semiconductor device as claimed in claim 21, wherein the column address

signal is generated in proportion to a value of the write recovery time.

23. The semiconductor device as claimed in claim 19, wherein the column address set signal is activated by the write enable signal and is deactivated after a predetermined delay time.

24. A method of controlling a semiconductor device, including a memory cell array consisting of a plurality of cell units, a bit line amplifier for amplifying a voltage difference between a bit line voltage and a complementary bit line voltage of the memory cell array, switching devices activated by a column selection line signal for electrically connecting a data line and a complementary data line to the bit line and the complementary bit line, respectively, and a write driver for supplying a write data voltage to the data line and the complementary data line, comprising the steps of:

writing data voltage into the memory cell array; and

generating the column selection line signal during a write recovery time.

25. The method as claimed in claim 24, wherein the step of generating the column selection line signal includes generating the column selection line signal repetitively.

26. The method as claimed in claim 25, wherein the step of generating the column selection line signal includes activating the column selection line signal using the write enable signal.

27. The method as claimed in claim 26, wherein the step of generating the column selection line signal includes generating the write enable signal during at least one clock of a master clock signal after a start of the write recovery time.

28. The method as claimed in claim 27, wherein the step of generating the column

selection line signal includes generating the write enable signal in proportion to a value of the write recovery time.

29. The method as claimed in claim 28, wherein the step of generating the column selection line signal includes deactivating the write enable signal using a stop signal of a column address burst counter.

30. The method as claimed in claim 29, wherein the step of generating the column selection line signal includes generating the stop signal of the column address burst counter with a delay by at least one clock of the master clock signal after a start of the write recovery time.

31. The method as claimed in claim 30, wherein the step of generating the column selection line signal includes generating the stop signal of the column address burst counter in proportion to a value of the write recovery time.